**[0015]** It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are not restrictive of this disclosure.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0016]** FIG. **1** is a circuit diagram illustrating the configuration of a protection circuit according to a first embodiment;

**[0017]** FIG. **2** is a circuit diagram illustrating the configuration of an electronic device including the protection circuit according to the first embodiment;

**[0018]** FIG. **3** is a vertical cross-sectional view illustrating the configuration of a thin film transistor with a double gate structure according to the first embodiment;

**[0019]** FIG. **4** is a circuit diagram illustrating a modification example of the protection circuit according to the first embodiment;

**[0020]** FIG. **5** is a vertical cross-sectional view illustrating a modification example of the thin film transistor with the double gate structure according to the first embodiment;

**[0021]** FIG. **6** is a circuit diagram illustrating the configuration of a protection circuit according to a second embodiment;

**[0022]** FIG. **7** is a graph illustrating the measurement result of a voltage (divided voltage) divided by thin film transistors according to the second embodiment;

**[0023]** FIG. **8** is a vertical cross-sectional view illustrating the configuration of a thin film transistor with an offset gate structure according to the second embodiment;

**[0024]** FIG. **9** is a circuit diagram illustrating a modification example of the protection circuit according to the second embodiment;

**[0025]** FIG. **10** is a vertical cross-sectional view illustrating a modification example of the thin film transistor with the offset gate structure according to the second embodiment;

**[0026]** FIG. **11** is a circuit diagram illustrating the configuration of a protection circuit according to a third embodiment; and

**[0027]** FIG. **12** is a circuit diagram illustrating a modification example of the protection circuit according to the third embodiment.

## DETAILED DESCRIPTION

**[0028]** Hereinafter, embodiments of the present disclosure will be described in detail with reference to the drawings.

### First Embodiment

**[0029]** Hereinafter, a first embodiment will be described.

**[0030]** In the specification and the claims, ordinal numbers, such as "first", "second", and "third", are given in order to clarify the relationship between elements and to prevent confusion between the elements. Therefore, the ordinal numbers do not limit the number of elements.

**[0031]** In addition, "connection" means electrical connection between connection targets. The "electrical connection" includes connection between the connection targets through an electrical element, such as an electrode, a wire, a resistor, or a capacitor. The "electrode" or the "wiring" does not functionally limit these components. For example, the "wiring" may be used as a portion of the "electrode". Inversely the "electrode" may be used as a portion of the "wiring".

**[0032]** FIG. **1** is a circuit diagram illustrating the configuration of a protection circuit **1**A according to this embodiment. FIG. **2** is a circuit diagram illustrating the configuration of an electronic device including the protection circuit **1**A according to the first embodiment. The protection circuit **1**A prevents an overvoltage which is caused by, for example, static electricity from being applied to an object to be protected.

**[0033]** As illustrated in FIG. **2**, the protection circuit **1**A is provided in an electronic device **2** including a device **7** to be protected, for example, a gate-in-panel (GIP) liquid crystal display (LCD) or a flat panel detector (FPD).

**[0034]** As illustrated in FIG. **1**, the protection circuit **1**A includes a control circuit **5** that controls current (hereinafter, referred to as "line current") between a first wiring **3** and a second wiring **4** and an application circuit **6** that applies a voltage to the control circuit **5**.

**[0035]** The first wiring **3** is a signal line to which, for example, an input voltage ($V_{IN}$) is applied and the second wiring **4** is a signal line to which a reference potential is applied. In this embodiment, the reference potential is, for example, a ground potential (GND). However, it is not limited thereto. The reference potential may not be the ground potential as long as it is lower than the potential of the first wiring **3**. In addition, the input voltage which is applied between the first wiring **3** and the second wiring **4** is referred to as a voltage between both ends of the protection circuit **1**A.

**[0036]** In this embodiment, when an overvoltage is applied to the first wiring **3**, the control circuit **5** operates such that current flows from the first wiring **3** to the second wiring **4** to protect the object to be protected from the overvoltage. Specifically, the control circuit **5** includes a thin film transistor Tr**1** that controls the line current.

**[0037]** The thin film transistor Tr**1** has a first electrode Tr**1***d* that is connected to the first wiring **3** and a second electrode Tr**1***s* that is connected to the second wiring **4**. The thin film transistor Tr**1** is an n-channel transistor. The first electrode Tr**1***d* functions as a drain electrode and the second electrode Tr**1***s* functions as a source electrode.

**[0038]** A gate electrode Tr**1***g* of the thin film transistor Tr**1** is connected to the application circuit **6** at a connection point **11**A.

**[0039]** The application circuit **6** includes a thin film transistor Tr**2** and a thin film transistor Tr**3** which are connected in series to each other.

**[0040]** A first electrode Tr**2***d* of the thin film transistor Tr**2** is connected to the first wiring **3**, and a second electrode Tr**2***s* of the thin film transistor Tr**2** is connected to a first electrode Tr**3***d* of the thin film transistor Tr**3**. A second electrode Tr**3***s* of the thin film transistor Tr**3** is connected to the second wiring **4**. The thin film transistors Tr**2** and Tr**3** are n-channel transistors. The first electrodes Tr**2***d* and Tr**3***d* function as drain electrodes and the second electrodes Tr**2***s* and Tr**3***s* function as source electrodes.

**[0041]** As illustrated in FIG. **3** which will be described below, the thin film transistors Tr**1**, Tr**2**, and Tr**3** are oxide semiconductor TFTs having an oxide semiconductor layer **22**.

**[0042]** Each of the thin film transistor Tr**2** and the thin film transistor Tr**3** is a transistor with a so-called double gate (dual gate) structure which has a bottom gate and a top gate.

**[0043]** That is, the thin film transistor Tr**2** includes a bottom gate electrode Tr**2***bg* and a top gate electrode Tr**2***tg*.